Dots for Multibus

RASTER GRAPHICS

P.O. BOX 23334 TIGARD, OREGON 97223 (503) 620-2241

MARCH 15, 1979
Mar 80

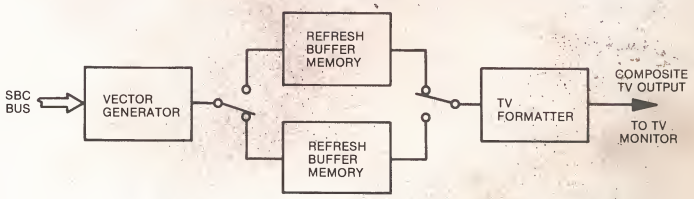
PRODUCT SPECIFICATION

RG-SBC 240 x 256 GRAPHICS GENERATOR

The RG-SBC 240x256 Graphics Generator is a versatile single board graphics generator designed for Intel's MULTIBUS*. It is easy to program and is ideal for creating moving displays requiring real time update. It contains a vector generator, provides its own refresh memories, and produces a composite TV signal that connects directly to a standard 525-line TV monitor.

FEATURES

- 240 x 256 Element Resolution
- Fast Vector Generator
- Dual Refresh Buffer Memories
- RS-170 Compatible TV Output
- Four Modes of Operation
- Simple Instruction Set



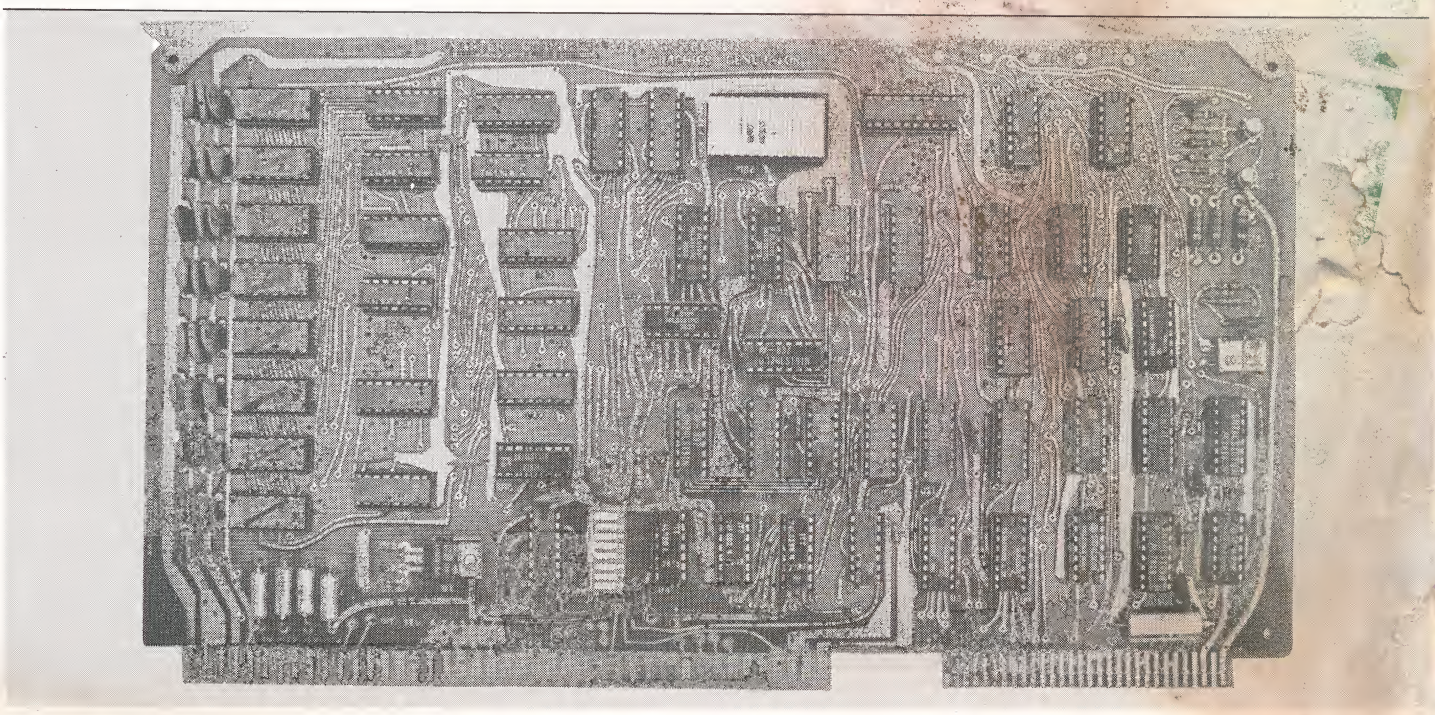
RG-SBC BLOCK DIAGRAM

DESCRIPTION

The RG-SBC 240x256 Graphics Generator includes a vector generator and dual refresh buffer memory on a single board. It plugs directly into the MULTIBUS* and appears as seven I/O ports for programming. A simple instruction set of only seven instructions allows fast, efficient programming in assembly language, BASIC, or other high-level language. Each instruction is a single byte written to a different I/O port within a user-selected I/O page.

The instructions are: X position, Y position, Vector length, Vector direction, Vector direction/length, Switch memories, and Mode select.

Programming is simple. Specify the starting location with a byte for X and a byte for Y. To create a small vector, then merely write one byte to the vector direction/length port. The vector generator starts automatically, issues a busy signal to the status port, and stops when the vector has been written into the refresh buffer memory.



*MULTIBUS is a trademark of Intel Corp.

The tasks of creating the vector, writing it into the refresh memory, and producing the TV signal are performed in hardware and are transparent to the user.

When the vector generator stops, the busy signal goes away. Another vector may then be created, continuing from where the last vector left off, in effect, "chaining" the vectors together.

Symbols, shapes, and patterns are easily created by "chaining" vectors together. An efficient one-byte vector direction/length instruction is provided for symbols composed of small vectors such as alphanumeric characters. Larger vectors may also be chained together; however, two bytes are required for programming, specifying length and direction.

Data written into the refresh memory is read by the TV formatter and converted into a composite TV signal for display on a standard 525-line TV monitor.

The user may display data from either refresh memory by issuing the switch command. The previously-displayed data may be optionally erased or retained when the memories are switched, thus providing stored or non-stored modes of operation.

New data may be written into either refresh memory, as determined by mode.

MODES OF OPERATION

Four modes of operation are possible, two stored modes and two erase modes.

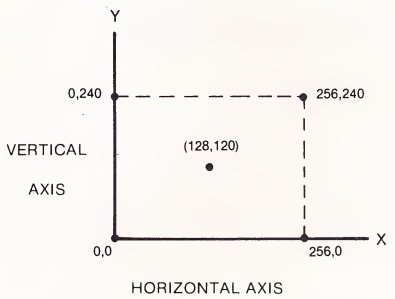
In the erase modes, data previously displayed is automatically erased when the refresh memories are switched.

In the stored modes, data is retained when the refresh memories are switched.

New data may optionally be written into either refresh memory, thus producing four modes of operation.

COORDINATE SYSTEM

A standard first quadrant cartesian coordinate system is used. All values are positive. For example, the display center is X = 128, Y = 120.



DISPLAY COORDINATE SYSTEM

VECTOR GENERATOR

The vector generator produces a variable length vector in one of eight directions. Two types of vectors are available for each mode:

ERASE MODE

Write Vector — Write vectors write 1s into memory.

No-Write Vector — No-Write vectors do not change the contents of memory but increment the address counters the same as Write Vectors.

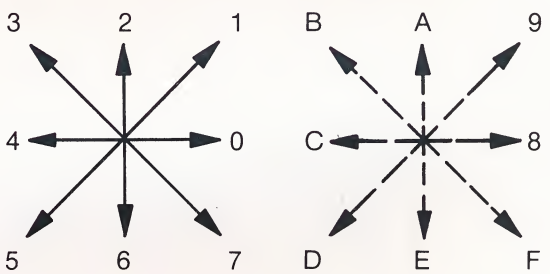
STORED MODE

Write Vector — Write Vectors write 1s into memory.

Erase Vector — Erase Vectors write 0s into memory

The length is specified with the length instruction and can be from 0 to 255 elements long. Alternately, the Direction/Length Instruction may be used for vectors up to 15 elements long.

Vector direction are specified by the 4 MSBS of the Vector Instruction, or by the 4 MSBS of the combined Length Instruction.



WRITE VECTORS

NO-WRITE VECTORS
OR
ERASE VECTORS

VECTOR TYPES WITH HEX CODING

The vector generator starts writing a vector at 1.6 usec/bit into the refresh buffer memory as soon as it receives the Direction Instruction, and stops when finished. Hence, instructions may be conveniently read from a table to produce complex displays.

This simple vector generator is extremely versatile because it is easy to program, may be efficiently used to create complex displays, and allows vector rotation with software.

In the erase mode, write vectors may be chained with no-write vectors to produce gaps in symbols.

In the stored mode, erase vectors allow selective erase.

VECTOR ROTATION

Vectors may be rotated in software to approximately 1.5 degrees resolution with supplied software.

DUAL REFRESH MEMORY

A unique and useful feature of the RG-SBC 240x256 Graphics Generator is the dual refresh memory. Each memory contains 240x256 elements, but data is displayed from only one buffer at a time.

The refresh memories are not in the processor address space and are only written to by the vector generator. However, every bit is singularly addressable by the vector generator.

Dual refresh memories are essential for complex moving displays, as they eliminate the objectionable read/write interference that occurs when data is written and read from the same memory. With dual memories a new display may be completely formed before it is displayed, thus providing an "instantaneous" shift from the old display to the new display. Some displays may take several TV fields to construct. In a single memory system, only part of the display would be constructed when the TV signal is produced, causing the displayed image to flicker and vary in intensity.

With Dual Refresh Memories data may be displayed from one refresh memory while a new display is being created in the other. When the new display is complete, the user may issue the switch command, which automatically switches the refresh memories, causing the new data to be displayed. Optionally, depending on the mode, the previously displayed data may be erased or retained when the memories are switched.

All synchronization is done in hardware, so the switch command may be issued at any time. Switching actually occurs at the end of the next complete TV field.

The processor memory is used only to store the instruction list, and not to perform any refresh function. Nor is DMA required. All communications to the graphics generator are with I/O instructions.

I/O ADDRESSING

The programming ports of the graphics generator reside in one page of I/O address space. A dip switch is provided to select the 1 of 16 I/O pages.

INSTRUCTIONS

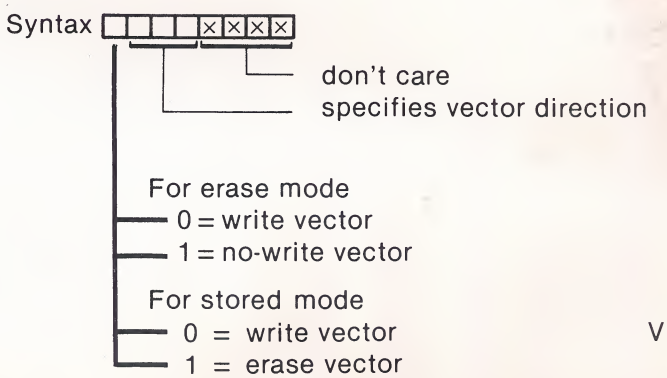
It is assumed that I/O page "C" HEX (1100) has been selected with the dip switch for the following discussion.

1. X Position: One byte written to I/O port C7H, range 0-255. Specifies the horizontal starting point for a vector.

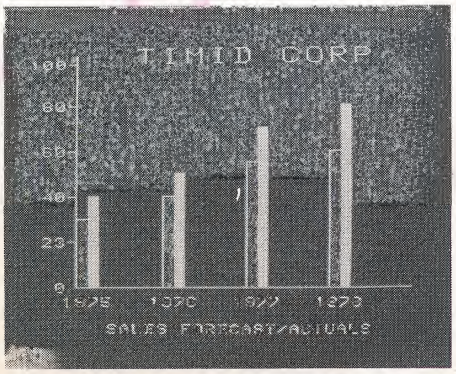
2. Y Position: One byte written to I/O port C6H, range 0-240. Specifies the vertical starting point for a vector.

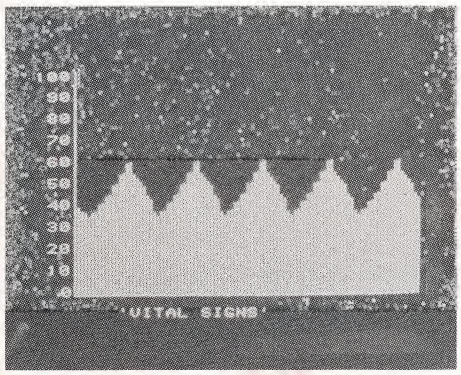
3. Vector Length: One byte written to I/O port C5H, range 0-255. Specifies vector length. A zero-length vector will write data at the present address but will not increment the address counters.

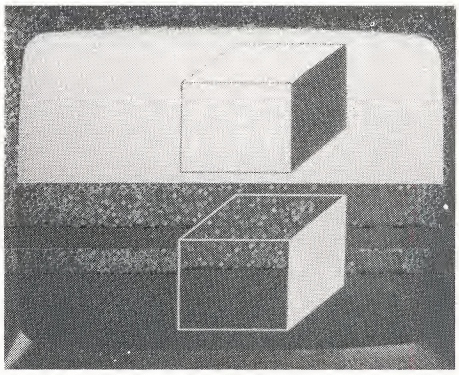
4. Vector Direction: One byte written to I/O port C4H. Specifies vector type and direction. Only the four MBSs are The vector generator starts with this instruction.

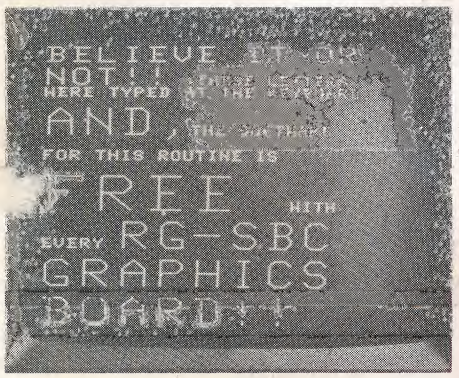


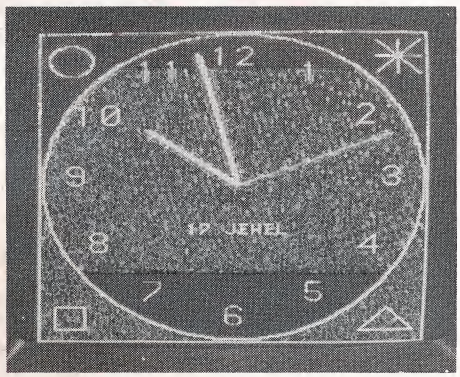
VECTOR DIRECTIONS & CODE

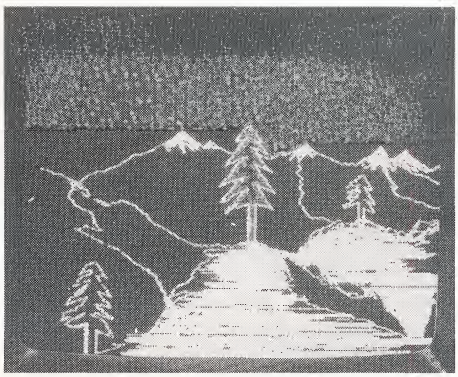

TIMID CORP
100
80
60
40
20
0
1975
1976
1977
1978
SALES FORECAST/ACTUALS

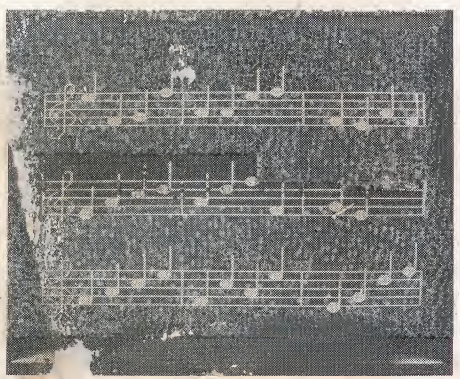

VITAL SIGNS

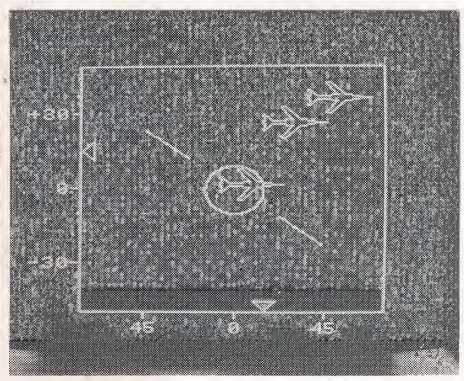


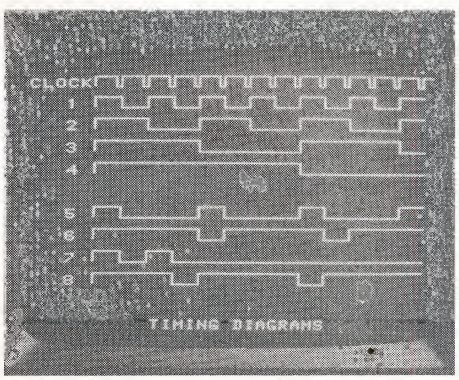

BELIEVE IT OR
NOT!!
WERE TYPED AT THE TERMINAL
AND, THE SOURCE
FOR THIS ROUTINE IS
FREE WITH
EVERY RG-SBC
GRAPHICS
BOARD!!

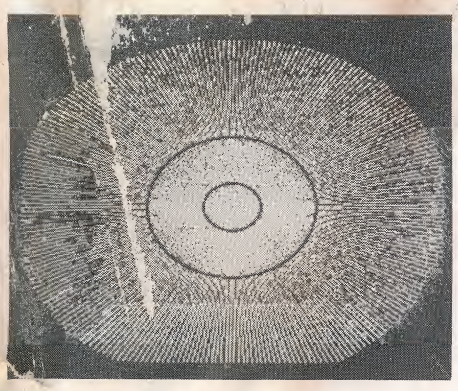

12
1
2
3
4
5
6
7
8
9
10
1P JEWEL

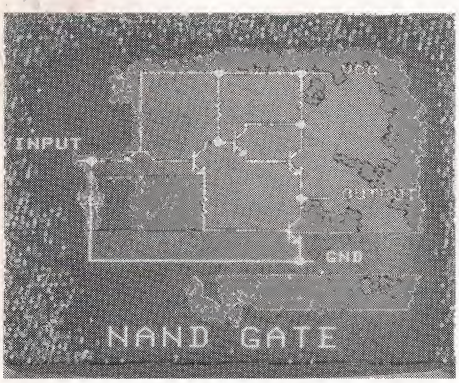


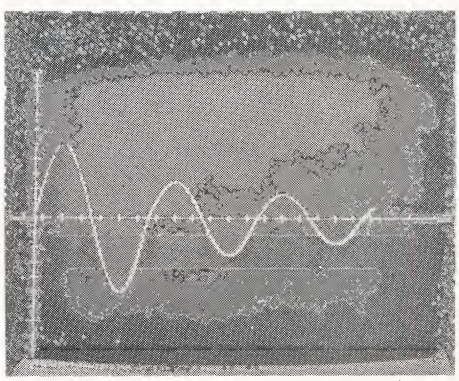


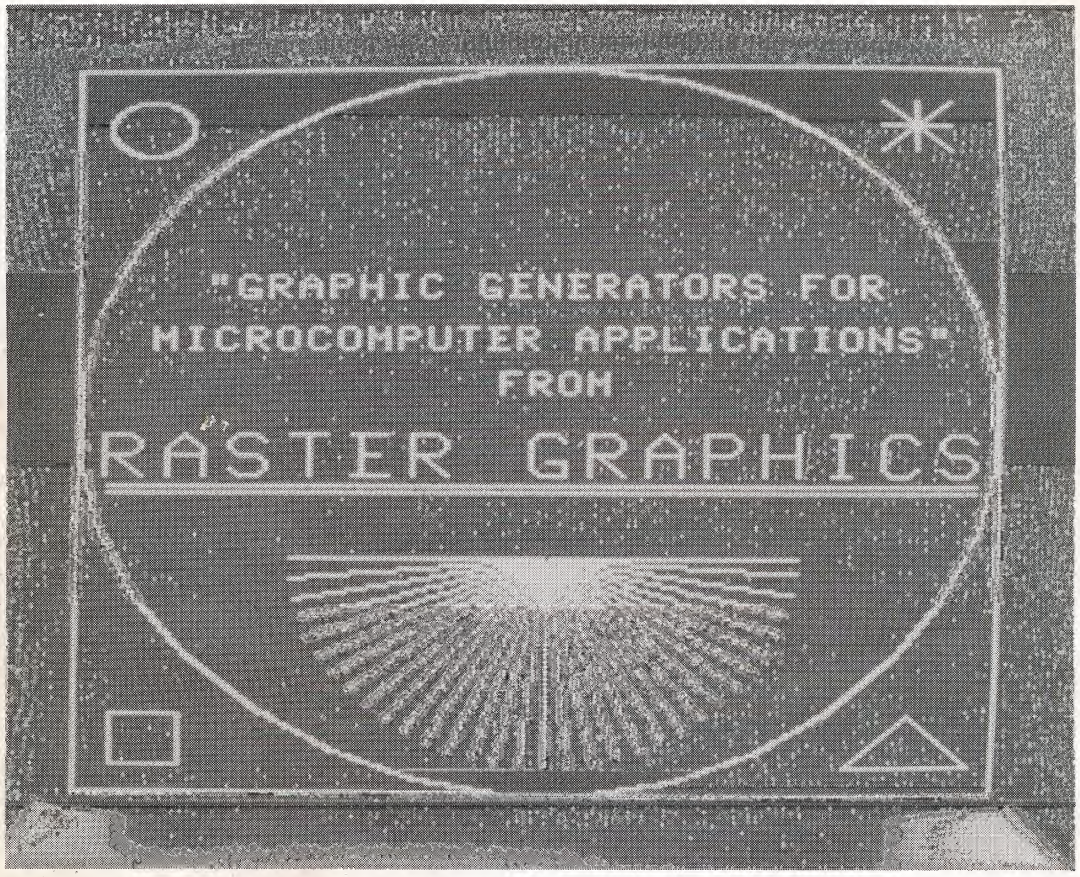

+80
0
-80
45
0
45


CLOCK
1
2
3
4
5
6
7
8
TIMING DIAGRAMS




INPUT
GND
NAND GATE





RAS[illegible] GRAPHICS
P.O. Box 23334
Tigard, Oregon 97223
(503) 620-2241

FIRST CLASS

Vectors for Multibus

RASTER GRAPHICS

P.O. BOX 23334 TIGARD, OREGON 97223 (503) 620-2241

July 15, 1979
Mar 80

PRODUCT SPECIFICATION

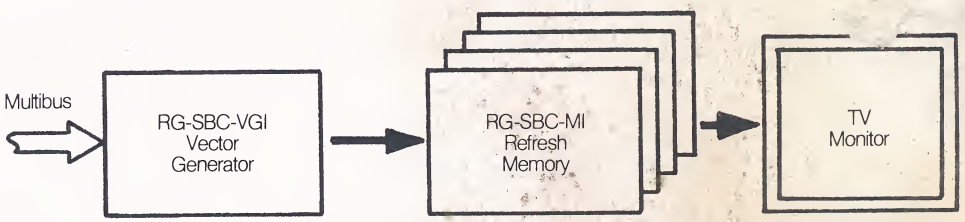
RG-SBC CONFIGURABLE GRAPHICS GENERATOR

The RG-SBC Configurable Graphics Generator is a high resolution graphics generator designed for Intel's Multibus. It consists of two boards, the RG-SBC-VGI Vector Generator and the RG-SBC-MI Refresh Memory. These two boards form a complete high resolution graphics generator which produces a composite TV signal for display on a standard TV monitor.

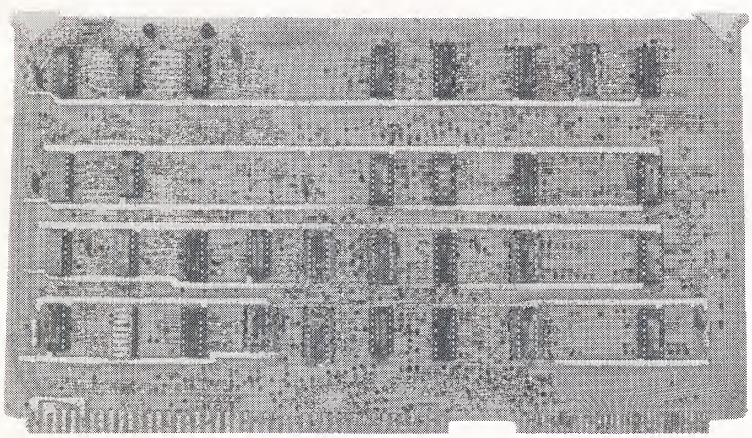
A single RG-SBC-VG1 Vector Generator may be combined with from one to eight RG-SBC-M1 Refresh Memory boards to produce high resolution black and white graphics, color graphics, or graphics with up to 16 shades of gray. The resolution may range from 320H x 240V to 640H x 480V, depending on the configuration. The Graphics Generator may be configured with dual refresh memories for dynamic displays applications requiring real time update, or with a single refresh memory, for high resolution static displays needs.

FEATURES

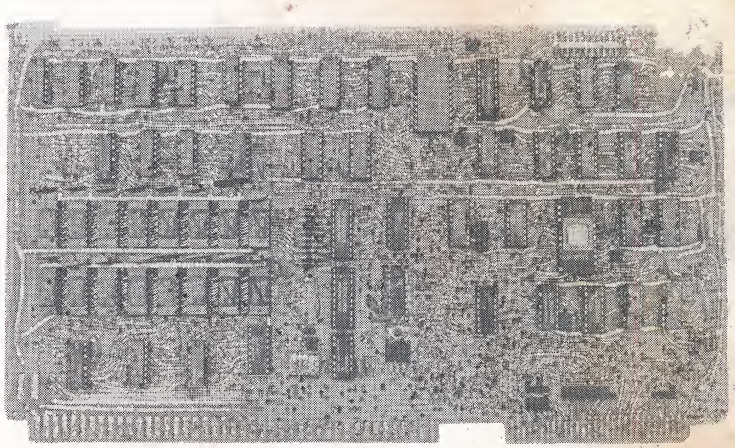
- **High Resolution Graphics**
  320H X 240V to
  640H X 480V
- **RGB Color Outputs**
- **Up to 16 Shades of Gray**
- **Sync to External TV**
- **525 TV, 60Hz/625 TV, 50Hz**
- **Single/Dual Refresh Memory**
- **Stored/Non-Stored Modes**
- **Selective/Screen Erase**
- **Composite TV Output Signal**
- **Separate TTL Level Outputs**
- **Simple Instruction Set**



RG-SBC Configurable Graphics Generator



RG-SBC-VG1 Vector Generator



RG-SBC-M1 Refresh Memory

Multibus is a trademark of Intel Corp.

DESCRIPTION

A simple instruction set controls the RG-SBC-VGI Vector Generator and allows the user to create vectors which are written into the RG-SBC-MI Refresh Memory. The instruction ports reside in one page of user selected I/O address space. Programming the Graphics Generator is simple. Specify the vector starting location with two bytes for X position and two bytes for Y position. Then, to create a small vector, merely write one byte to the Vector Direction/Length I/O port. The vector generator starts automatically, issues a busy signal to the status port, and stops when the vector has been written into the refresh memory.

The task of creating the vector, writing it into the refresh memory, and producing the TV signal are performed with hardware and are transparent to the user.

When the vector generator stops, the busy signal is removed. Another vector may then be created by merely writing another byte to Vector Direction/Length I/O port. This second vector will continue from where the first vector left off, in effect, "chaining" the vectors together.

Symbols, shapes and patterns are easily created by "chaining" vectors together. An efficient one-byte Vector Direction/Length instruction is provided for symbols composed of small vectors such as alphanumeric characters. Larger vectors may also be "chained" together; however, two bytes are required for programming, specifying length and direction. Data written into the refresh memory is automatically converted into a composite TV signal for display on a standard 525-line TV monitor, or optionally, on a 625-line TV monitor.

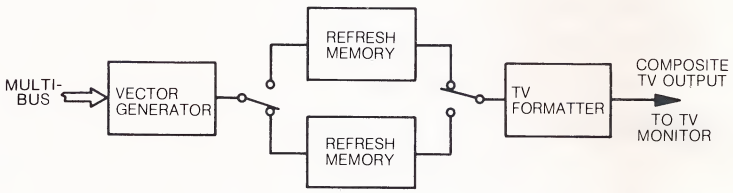
With dual refresh memory configurations, the user may display data from either refresh memory by merely issuing the switch command. The previously displayed data may be optionally erased or retained when the memories are switched, thus providing stored and non-stored modes of operation.

REFRESH MEMORY CONFIGURATION

The graphics generator may be configured with either dual or single refresh memories.

Dual Refresh memories are essential for complex moving displays as they eliminate the objectionable read/write interference that occurs when data is written and read from the same memory. With dual refresh memories a new display may be completely formed before it is displayed, thus providing an "instantaneous" shift from the old display to the new display.

Single refresh memory configurations are useful for display formats that are updated infrequently, or where higher resolution is required, using all the available memory. Refresh memories are not in the processor address space and are only written to by the vector generator. However, every bit is addressable.



Dual Refresh Memory Configuration

Single Refresh Memory Configuration

MODES OF OPERATION

Stored and non-stored modes of operation are available. For dual refresh memory configurations, two stored and two erase modes are available. For single refresh memory configurations, one stored mode and one erase mode are available.

Erase Mode

In the erase mode,data previously displayed is automatically erased when the switch command is issued. For dual refresh memory configurations, issuing the switch command causes data to be displayed from the other refresh memory. Data previously displayed is erased. Either refresh memory may be selected for update, thus producing two non-stored modes of operation.

For single refresh memory configurations, issuing the switch command causes the refresh memory to be erased.

Two vector types are available in the erase mode, write and no-write vectors.

The erase procedure is synchronized to the TV field with hardware, so the switch command may be issued at any time.

Stored Mode

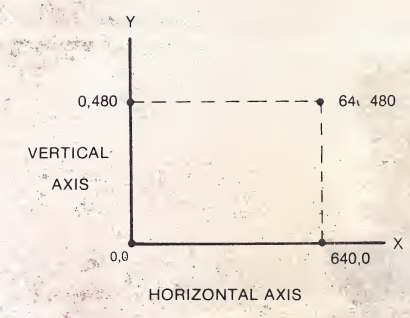
For dual refresh memory configurations and when in the stored mode, issuing the switch command causes the refresh memories to be switched, but data previously displayed is retained. Issuing the switch command has no effect on single refresh memory configurations.

I/O Addressing

Instruction and status ports for the RG-SBC-VGI Vector Generator reside in one page of user selected I/O address space. A dip switch is provided to select the 1 of 16 I/O pages.

Coordinate System

A standard first quadrant cartesian coordinate system is used. All values are positive. Coordinate limits depend on the refresh memory configuration.



DISPLAY COORDINATE SYSTEM

Vector Generator

The vector generator produces a variable length vector in one of eight directions. Two types of vectors are available for each mode:

ERASE MODE

1. Write Vector	Write Vectors write 1s into memory.
2. No-Write Vectors	No-Write vectors do not change the contents of memory but increment the address counters the same as Write Vectors.

STORED MODE

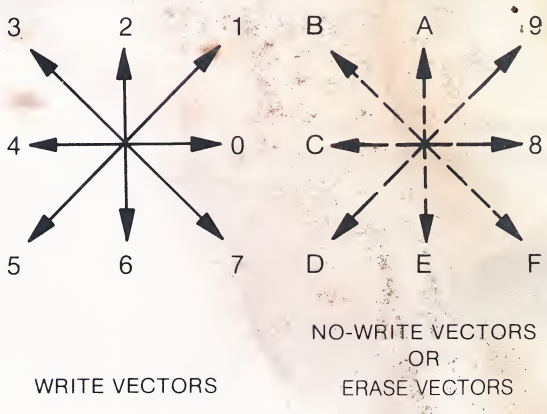
1. Write Vector	Write Vectors write 1s into memory.
2. Erase Vectors	Erase Vectors write 0s into memory.

The vector length is specified with the length instructions and may range from 0 to 4096 elements long. Alternately, the combination Direction/Length Instruction may be used to specify vectors up to 15 elements long.

Vector type and direction are specified by the 4 MSBS of the Vector Direction Instruction, or by the 4 MSBS of the combination Vector Direction/Length Instruction.

The vector generator starts writing a vector at about 2 usec/bit into the refresh memory as soon as it receives the Direction Instruction, and stops when finished. Hence, instructions may be conveniently read from a table to produce complex displays.

This simple vector generator is extremely versatile because it is easy to program, may be efficiently used to create complex displays, and allows vector rotation with software.



VECTOR TYPES WITH HEX CODING

OUTPUT SIGNAL

A composite TV signal producing 1.0V of video into 75 ohms is output. An interlaced or non-interlaced signal is generated depending on the vertical resolution. An RS-170 compatible signal is generated for 525 line TV and a similar signal is generated for 625 line TV.

SYNCHRONIZING TV SIGNALS

When more than one RG-SBC-M1 Refresh Memory is used, the video from each board is combined into one composite TV signal for display on a standard TV monitor.

EXTERNAL SYNC

External sync pulses may be applied to the RG-SBC-M1 Refresh Memory synchronizing it with an external TV signal for applications requiring video mixing such as superimposing symbology on TV video.

RGB COLOR OUTPUTS

Three RG-SBC-M1 Refresh Memory boards may be configured to produce red, green, and blue outputs for color monitors accepting TTL level RGB inputs.

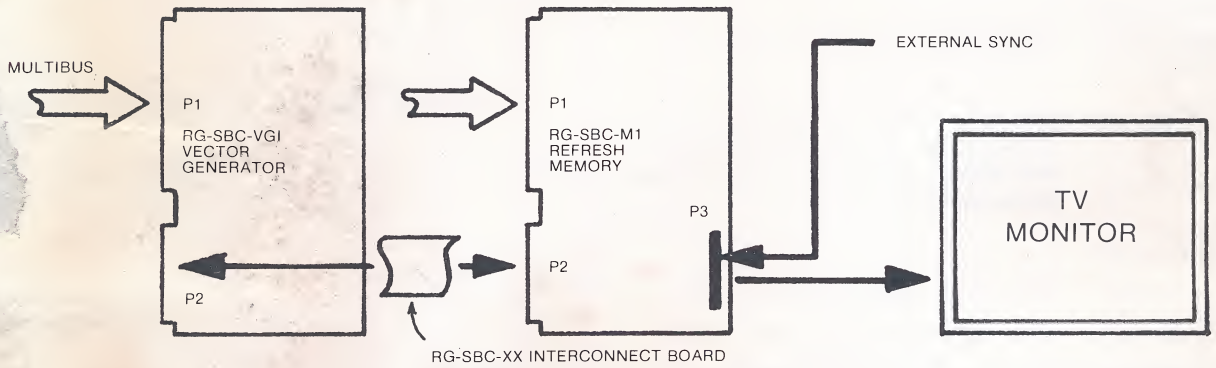
PROGRAMMING IN BASIC

Complex displays may easily be programmed in BASIC. Merely calculate the X and Y coordinates of the desired shape, scale them appropriately, and send the coordinates to the graphics generator a point at a time. After each pair of coordinates has been transferred, output a vector of zero length to write the coordinates into memory.

PHYSICAL CONFIGURATION

The Multibus interfaces directly to the RG-SBC-VGI Vector Generator via the 86 pin connector PI. The RG-SBC-M1 Refresh Memory acquires only power from PI. Connections between the RG-SBC-VGI Vector Generator and the RG-SBC-M1 Refresh Memory are made via the 60 pin connector P2. A small interconnect board is provided for this purpose.

The composite TV signal is made available at P2 and at the top of the RG-SBC-M1 Refresh Memory board. TTL level horizontal blank, vertical blank, and video are also made available at the top of the board, at connector P3.
External sync signals are connected via the connector, P3, at the top of the RG-SBC-M1 Refresh Memory board.



Interconnection Block Diagram

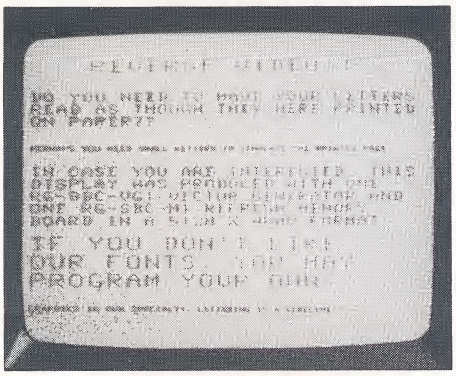
RG-SBC-XX INTERCONNECT BOARD

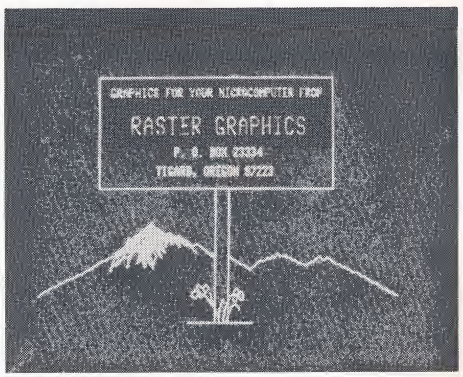
This board is used to connect the RG-SBC-VGI Vector Generator to the RG-SBC-M1 Refresh Memory. An interconnect board with the proper number of connectors is required for each configuration. The connectors are on .75 inch centers. Other center to center dimensions may be special ordered. The dash number indicates the number of connectors.

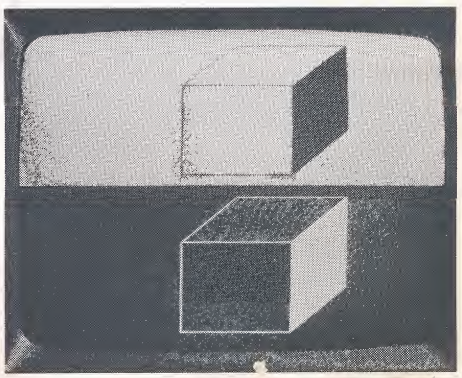
POWER REQUIREMENT

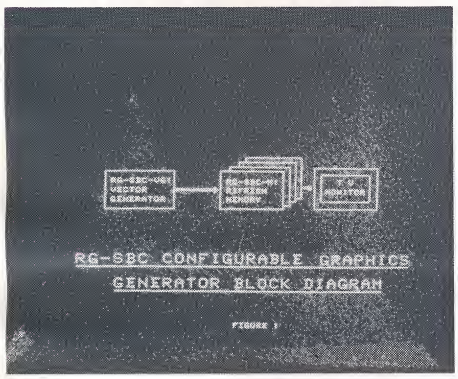
RG-SBC-VG1 Vector Generator	+ 5VDC	@	.4a
RG-SBC-M1 Refresh Memory	+ 12VDC	@	.4a
	+ 5VDC	@	1.0a
	- 5VDC	@	.1a

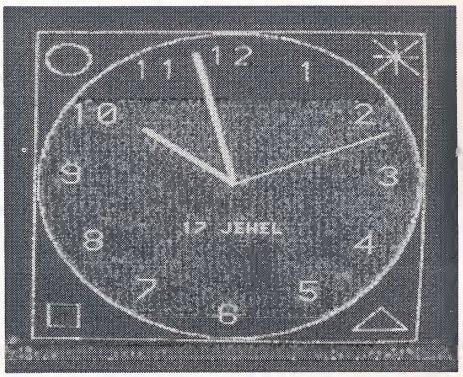
NOTE: A-5V regulator is provided to generate-5V from-12V for MDS-800 and SERIES II applications. A jumper is required to connect the output of the regulator to the-5V bus.

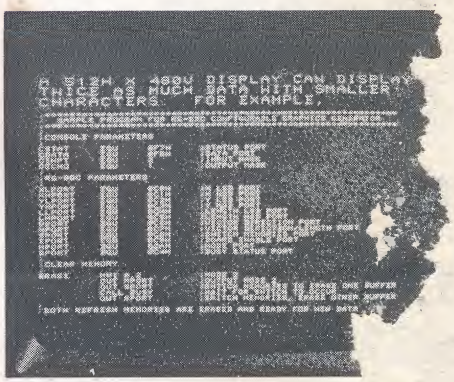

DO YOU NEED TO HAVE YOUR LETTERS
READ AS THOUGH THEY WERE PRINTED
ON PAPER?
IN CASE YOU ARE INTERESTED, THIS
DISPLAY WAS PRODUCED WITH ONE
RG-SBC-VG1 VECTOR GENERATOR AND
ONE RG-SBC-M1 REFRESH MEMORY
BOARD IN A 512H X 480V FORMAT.
IF YOU DON'T LIKE
OUR FONTS, YOU MAY
PROGRAM YOUR OWN.

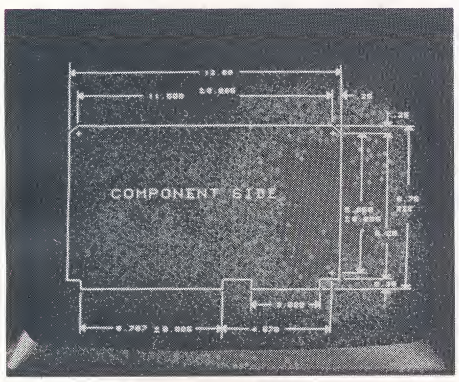

GRAPHICS FOR YOUR MICROCOMPUTER FROM
RASTER GRAPHICS
P. O. BOX 23234
TIGARD, OREGON 97223

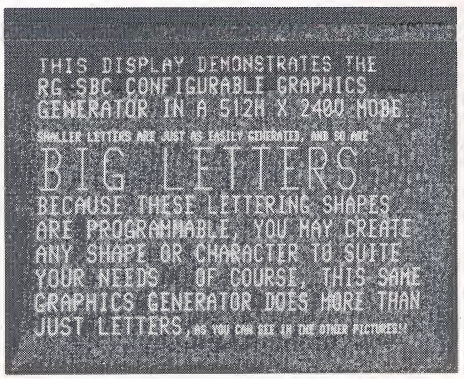


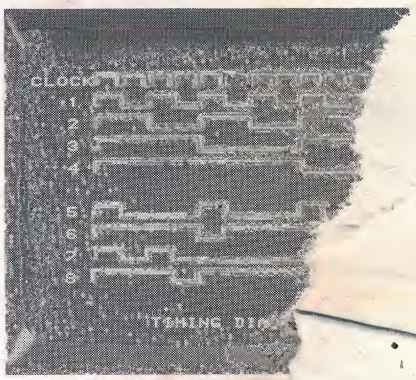

RG-SBC CONFIGURABLE GRAPHICS
GENERATOR BLOCK DIAGRAM

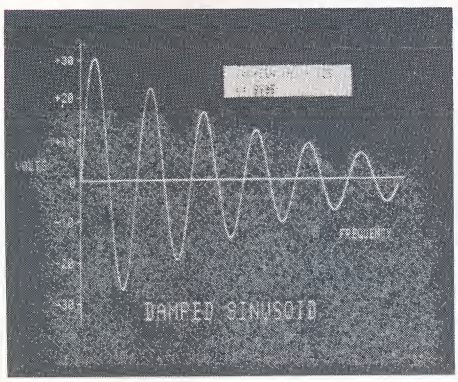

17 JEWEL

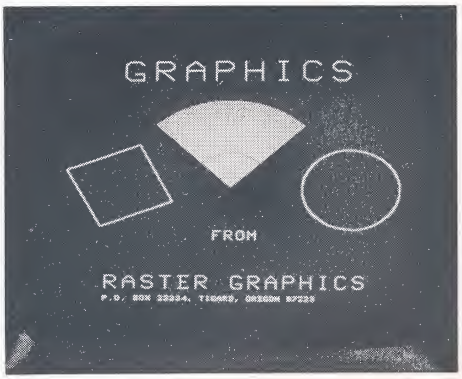

A 512H X 480V DISPLAY CAN DISPLAY
TWICE AS MUCH DATA WITH SMALLER
CHARACTERS. FOR EXAMPLE,

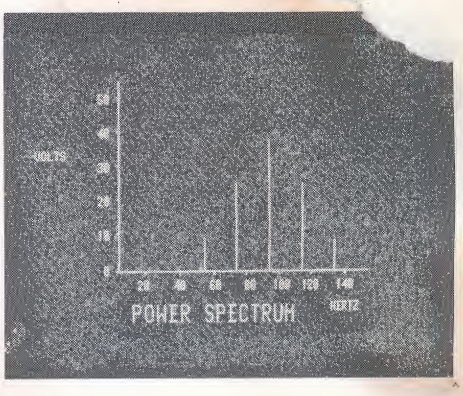

COMPONENT SIDE


THIS DISPLAY DEMONSTRATES THE
RG-SBC CONFIGURABLE GRAPHICS
GENERATOR IN A 512H X 240V MODE.
SMALLER LETTERS ARE JUST AS EASILY GENERATED, AND SO ARE
BIG LETTERS.
BECAUSE THESE LETTERING SHAPES
ARE PROGRAMMABLE, YOU MAY CREATE
ANY SHAPE OR CHARACTER TO SUITE
YOUR NEEDS. OF COURSE, THIS SAME
GRAPHICS GENERATOR DOES MORE THAN
JUST LETTERS, AS YOU CAN SEE IN THE OTHER PICTURES!!


CLOCK

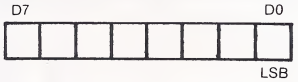
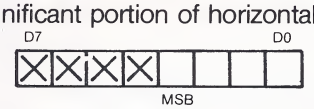
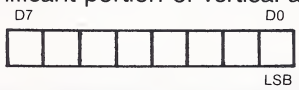
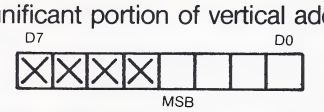
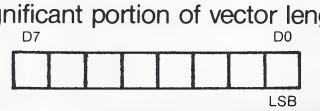
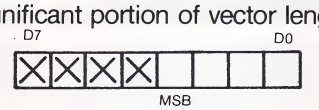
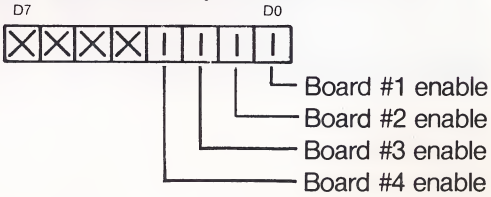

DAMPED SINUSOID

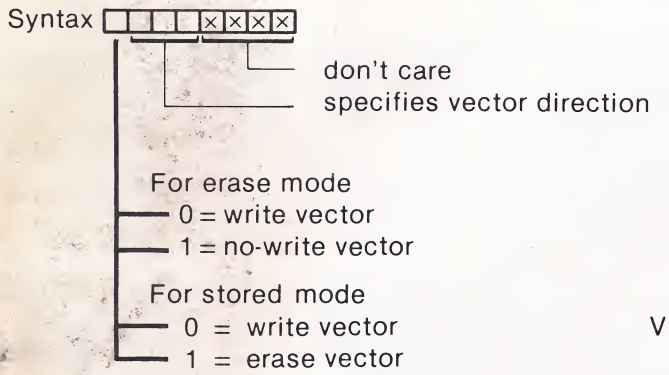

GRAPHICS
FROM
RASTER GRAPHICS

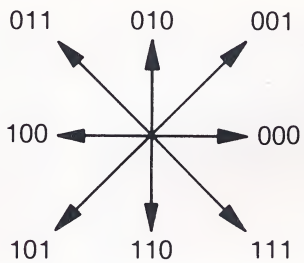

VOLTS
KHTZ
POWER SPECTRUM

INSTRUCTIONS

It is assumed, for the following discussion, that I/0 port "C" HEX (1100) has been selected with the dip switch. Each instruction is written to its own I/0 port as specified.

INSTRUCTION BYTE	I/0 PORT	DESCRIPTION
X Position	C0	Least significant portion of horizontal address. Syntax 
X Position	C1	Most significant portion of horizontal address. Syntax 
Y Position	C2	Least significant portion of vertical address. Syntax 
Y Position	C3	Most significant portion of vertical address. Syntax 
ector Length	C4	Least significant portion of vector length. Syntax 
Vector Length	C5	Most significant portion of vector length. Syntax 
V r Direction	C6	Specifies vector type and direction. Only the 4 MSBs are used. The vector generator starts with this instruction.
Vector Direction/Length	C7	The 4 MSBs specify the vector type and direction the same as the Vector Direction instruction. The 4 LSBs specify the vector length, range 0-15. The vector generator starts with this instruction.
Switch Refresh Memories	C8	Any data written to I/0 port C8. Switches refresh memories. Data previously displayed is erased in the erase mode. Busy status is indicated during the switching process.
Board Enable	C9	Enables the Refresh Memory to recieve new data. Syntax 





VECTOR DIRECTIONS & CODE

INSTRUCTION BYTE	I/0 PORT	DESCRIPTION
Mode Select	CA	Selects stored or erase mode.
		
Mode 0	0 0	Stored Mode. For dual refresh memory configurations, new data is written into the alternate refresh memory. Data previously displayed is retained when the switch command is issued. For single refresh memory configurations, this mode allows use of write and erase vectors for selective erase. The switch command is not used.
Mode 1	0 1	Stored Mode. For dual refresh memory configurations, new data is written into the displayed refresh memory. Data previously displayed is retained when the switch command is issued. For single refresh memory configurations, thi mode allows use of write and erase vectors for selective erase. The switch command is not used.
Mode 2	1 0	Erase Mode. For dual refresh memory configurations, new data is written in the alternate memory. Data previously displayed is erased when the switch command is issued. For single refresh memory configurations, t refresh memory is erased when the switch command is issued.
Mode 3	1 1	Erase Mode. For dual refresh memory configurations, new data is written into the displayed refresh memory. Data previously displayed is erased when the switch command is issued. For single refresh memory configurations, the refresh memory is erased when the switch command is issued.

Status Information

X Position	C0	Reads the 8 LSBs of the Vector Generator's horizontal address counter.
X Position	C1	Reads the 4 MSBs of the Vector Generator's horizontal address counter.
Y Position	C2	Reads the 8 LSBs of the Vector Generator's vertical address counter.
Y Position	C3	Reads the 4 MSBs of the Vector Generator's vertical address counter.
Busy	C4	MSB=0 if the Vector Generator is busy or if the refresh memories are being switched. MSB=1 if the new instructions may be sent to the Vector Generator.

CONFIGURABLE GRAPHICS GENERATOR CONFIGURATION SUMMARY

625 Line TV, 50Hz		525 Line TV, 60Hz		Video Levels	Interlace Yes/No	Number of Refresh Memories	Number of Boards required		RG-SBC-XX Interconnect Board	Configuration Price
Configuration Number	Display Resolution	Configuration Number	Display Resolution				RG-SBC-VG1 Vector Generator	RG-SBC-M1 Refresh Memory		
E1-2	341H x 256V	1-2	320H x 240V	2	no	2	1	1	–02	$ 995
E1-4	341H x 256V	1-4	320H x 240V	4	no	2	1	2	–03	1780
E1-8	341H x 256V	1-8	320H x 240V	8	no	2	1	3	–04	2565
E1-16	341H x 256V	1-16	320H x 240V	16	no	2	1	4	–05	3350
E2-2	512H x 256V	2-2	512H x 240V	2	no	2	1	1	–02	995
E2-4	512H x 256V	2-4	512H x 240V	4	no	2	1	2	–03	1780
E2-8	512H x 256V	2-8	512H x 240V	8	no	2	1	3	–04	2565
E2-16	512H x 256V	2-16	512H x 240V	16	no	2	1	4	–05	3350
E3-2	512H x 512V	3-2	512H x 480V	2	yes	1	1	1	–02	995
E3-4	512H x 512V	3-4	512H x 480V	4	yes	1	1	2	–03	1780
E3-8	512H x 512V	3-8	512H x 480V	8	yes	1	1	3	–04	2565
E3-16	512H x 512V	3-16	512H x 480V	16	yes	1	1	4	–05	3350
E4-2	512H x 512V	4-2	512H x 480V	2	yes	2	1	2	–03	1780
E4-4	512H x 512V	4-4	512H x 480V	4	yes	2	1	4	–05	3350
E4-8	512H x 512V	4-8	512H x 480V	8	yes	2	1	6	–07	4920
E4-16	512H x 512V	4-16	512H x 480V	16	yes	2	1	8	–09	6490
E5-2	682H x 512V	5-2	640H x 480V	2	yes	1	1	2	–03	1780
E5-4	682H x 512V	5-4	640H x 480V	4	yes	1	1	4	–05	3350
E5-8	682H x 512V	5-8	640H x 480V	8	yes	1	1	6	–07	4920
E5-16	682H x 512V	5-16	640H x 480V	16	yes	1	1	8	–09	6490
E1C-2*	341H x 256V	1C-2*	320H x 240V	2	no	2	1	3	–04	2565

*Three synchronized TTL level signals are provided for color monitors accepting RGB inputs.

INDIVIDUAL BOARD PRICES

		Price
RG-SBC-VG1	Vector Generator	$195
RG-SBC-M1	Refresh Memory	$775
RG-SBC-02	Interconnect Board	*$ 25

*Add $10.00 for each additional connector.
Dash number specifies the number of connectors.

ORDERING INFORMATION

Boards may be ordered individually or from the configuration summary above.

The Configurable Graphics Generator is fully socketed, burned-in, tested, and carries a 90 day warranty on parts and labor. A user manual is included.

Please order directly from:

Raster Graphics
P.O. Box 23334
Tigard, Oregon 97223